Atty. Dkt. No. 037267-0135

Replacement #15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Takaaki NAGAI et al.

Title: EEPROM SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

Appl. No.: 09/606,159

Filing Date: 06/29/2000

Examiner: P. Brock, II

Art Unit: 2815

MARK-UP VERSION OF AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed May 11, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please enter the following amended claims:

21. (Twice Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and perpendicular to a later formed plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon ~~layers~~strips in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon ~~layer~~ strips to thereby form said plurality of word lines, each word line having a plurality of ~~a~~ control gates and ~~a~~ floating gates;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(g') forming contact-holes through said first interlayer insulating layer only above both said drain and source regions in said plurality of memory cell transistors;

(h) forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said plurality of word lines and connecting source regions to one another and a plurality of bit studs extending to said drain regions;, said first metal wiring layer being formed above a surface of said first interlayer insulating layer;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a bit line extending perpendicularly to said plurality of word lines and connecting said drain regions with each other, said bit line having a top portion and a bottom portion with said top portion being wider than said bottom portion,

wherein said bottom portion of said bit line is connected to ~~said~~ a top portion of said plurality of bit studs and ~~said~~ a bottom portion of said plurality of bit studs is connected to said drain regions.

24. (Twice Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and

perpendicular to a later formed plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon ~~layers~~strips in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said plurality of first polysilicon ~~layer~~ strips to thereby form said plurality of word lines, each word line having a plurality of ~~a~~ control gates and ~~a~~ floating gates;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(g') forming contact-holes through said first interlayer insulating layer only above both said drain and source regions in said plurality of memory cell transistors;

(h) forming a first metal wiring layer which is patterned so as to form both a bit line connecting said drain regions to one another, and a plurality of source studs extending in parallel with said plurality of word lines, said plurality of source studs connecting to said source regions, said plurality of source studs having a top portion and a bottom portion with said top portion of said plurality of source studs being wider than said bottom portion of said plurality of source studs, said first metal wiring layer being formed above a surface of said first interlayer insulating layer;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other, said common source line having a top portion and a bottom portion with said top portion of said common source line being wider than said bottom portion of said common source line,

wherein said bottom portion of said common source line is connected to said top portion of said plurality of source studs and said bottom portion of said plurality of source studs is connected to said source regions.